Large-Signal Technique for Designing Single-Frequency and Voltage-Controlled GaAs FET Oscillators

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Abstract—**A systematic procedure is described for designing fixed-frequency and voltage-tuned GaAs FET oscillators for optimum large-signal performance. The approach is based on the use of a large-signal FET model for de-embedding dominant device nonlinearities, leading to a method which is both accurate and simple to apply. The viability of the technique is demonstrated with a 17-GHz fixed-frequency oscillator and a 7.4 to 13.1-GHz varactor-tuned oscillator. Design considerations as well as measured performance characteristics are discussed in detail.**

I. Introduction

Continuing efforts to improve GaAs FET performance characteristics have predominantly been focused on amplifiers for both low-noise and high-power systems applications at increasingly higher microwave frequencies. The GaAs FET is also an attractive candidate for use in efficient microwave oscillators, including broad-band tunable sources. From the point of view of nonlinear device operation, the two types of circuits are quite similar. Thus, except for a few secondary aspects, device technology and device characterization techniques developed for amplifier purposes can be readily carried over to meet GaAs FET oscillator design needs as well.

Prior to the development of methods for describing and predicting large-signal GaAs FET behavior, oscillator designs have relied chiefly on small-signal criteria. Although these criteria generally lead to accurate predictions of oscillating frequency, they are of limited value when it comes to optimizing efficiency and RF output power performance. To cope with this difficulty, methods [1], [2] based on so-called large-signal device S-parameters have been proposed. The large-signal S-parameters provide a linearized description of fundamental frequency device–circuit interaction at elevated drive levels for device terminating impedances in the vicinity of those prevailing during measurement (typically 50 Ω). The amount of error inherent in the approximation becomes increasingly significant, the further the actual terminations deviate from their 50-Ω reference value. This is easily visualized with the help of a simple device model containing third-order nonlinearities [3]. In a practical oscillator design, where there are no predetermined bounds on the values the actual terminating impedances can assume, the viability of the large-signal S-parameter approach thus becomes questionable.

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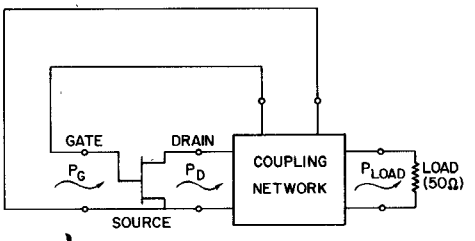

Fig. 1. GaAs FET oscillator.

Recently, a new method [4], [5] has been outlined which is aimed at overcoming previous limitations. It relies on a large-signal device model for de-embedding the dominant nonlinearities, leading to an exceptionally simple formulation of the optimum conditions for oscillation, while maintaining accuracy in predicting large-signal oscillator performance. This paper presents a comprehensive description of the technique and its experimental verification, supplying the details necessary to apply the method and to judge its reliability in assessing large-signal oscillator behavior. The general design approach for fixed-frequency oscillators is discussed in Section II, followed by the experimental verification thereof with a 17-GHz oscillator circuit in Section III. The application of the technique to voltage-controlled oscillators is described in Section IV, with an example of a VCO, tunable from 7.4 to 13.1 GHz, presented in Section V.

II. Design of Fixed-Frequency Oscillators

A. Basic Requirements for Achieving Optimum Oscillator Performance

The task of designing a transistor oscillator may be portrayed as that of synthesizing a three-port lossless coupling network (Fig. 1) which 1) yields a single stable state of oscillation, and 2) delivers maximum RF output power to an external (50-Ω) load for given bias conditions.

Approaches for satisfying the first constraint are relatively straightforward and are primarily concerned with parasitic oscillations and hysteresis effects. Spurious oscillations caused by parametric phenomena are normally absent in GaAs FET circuits, due to the dominance of resistive-type nonlinearities in the device. Consequently, states of oscillation and potential hysteresis effects can be checked out in the frequency domain [6] by recording

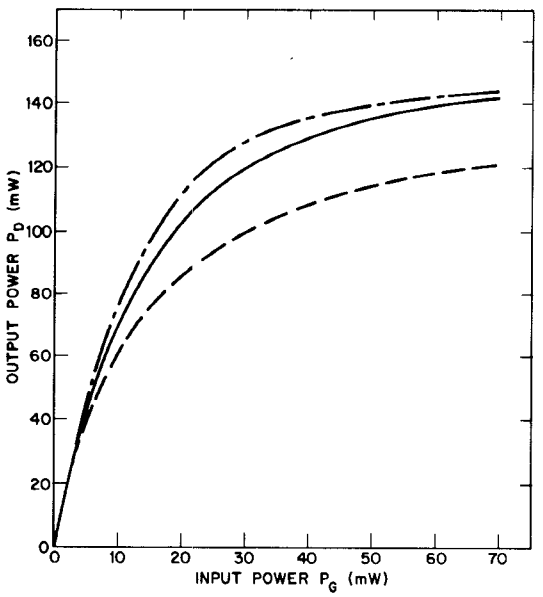

Fig. 2. Measured and approximated saturation characteristics for a single cell of an Avantek M110 GaAs FET at 8.5 GHz. _____ measured. ---- approximation (3). — · — · — approximation (4).

series and parallel system resonances under small-signal conditions, and then determining which of them—besides the one associated with the principal state of oscillation—might cause trouble. A conservative assessment is often appropriate in anticipation of circuit tolerances and spreads in device characteristics.

An obvious precaution is to choose coupling network configurations with minimum complexity in order to avoid, a priori, unnecessary resonances. This pertains especially to ones close to the principal frequency of oscillation. To suppress parasitic oscillations more remote from the principal frequency, additional stabilizing elements might be required. In single-frequency oscillators this can normally be achieved by augmenting the bias circuitry with lumped *RLC* elements, strategically placed so as not to interfere with RF output power performance.

Measures directed at satisfying the second constraint on the three-port coupling network (maximizing output power) are more complex and are the main topic of this paper. The general problem is to derive a systematic procedure for defining and implementing the optimum device terminating impedances and drain-to-gate feedback that produce maximum RF output power, P_{load}, while oscillating at only one frequency. For a lossless coupling network

$$P_{\text{load}}(\omega_0)=\max\{P_D(P_G,\omega_0)-P_G(\omega_0)\} \tag{1}$$

with P_D the RF power delivered by the transistor to its drain termination (Fig. 1), and P_G the power fed back into the gate port of the device to sustain oscillation at the angular frequency ω_0. With reference to the basic oscillation requirement for establishing resonance at ω_0, fundamental frequency *large-signal conjugate matching conditions* at both ports of the device are hereby implied for every pair of values (P_D, P_G). Equivalent to (1) is the familiar condition

$$\left.\frac{\partial P_D(P_G,\omega)}{\partial P_G(\omega)}\right|_{\omega=\omega_0}=1. \tag{2}$$

To find the solution satisfying (2), the device saturation characteristics $P_D(P_G,\omega_0)$ must first be determined. The most direct approach is to acquire the data through measurement. This is a straightforward but relatively inconvenient task, provided a large-signal setup is available. In an attempt to circumvent the inconvenience associated with such measurements, the use of suitable approximations will be explored in this paper for describing saturation characteristics and determining optimum load conditions.

B. Empirical Description of Device Nonlinear Characteristics

With respect to the saturation function $P_D(P_G,\omega_0)$ two analytical approximations proposed in the recent literature [7], [2] are

$$P_D(\omega_0)=\left(\frac{1}{P_G(\omega_0)\cdot\tilde{\Gamma}(\omega_0)}+\frac{1}{P_{D\max}}\right)^{-1} \tag{3}$$

$$P_D(\omega_0)=P_{D\max}\cdot\left\{1-\exp\left(-\tilde{\Gamma}(\omega_0)\cdot\frac{P_G(\omega_0)}{P_{D\max}}\right)\right\} \tag{4}$$

with $P_{D\max}$ the *maximum* achievable saturated output power for given bias conditions, and $\tilde{\Gamma}$ the *small-signal* maximum available power gain for the device in common source configuration. (Throughout this paper, the tilde is used to mark small-signal quantities.) As an illustrative example, Fig. 2 compares measured characteristics with those predicted from (3) and (4) for the 0.5-μm Avantek device used in experimental circuits described later on. The values provided by (4) are especially attractive, exhibiting a maximum deviation of less than 0.5 dB across the entire dynamic range. Equally good agreement has also been observed with devices from other manufacturers, such as with Texas Instruments 1.0-μm and 1.7-μm gate length devices [8], suggesting a more general applicability of (4) to

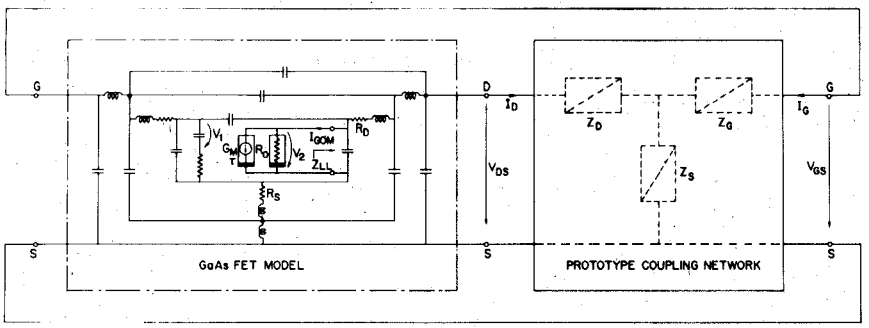

Fig. 3. Oscillator circuit with model of GaAs FET and two-port prototype of three-port coupling network.

GaAs FET's as a whole. Hence, (4) has been adopted as a viable approximation for use with in the present approach.

With $\tilde{\Gamma}(\omega_0)$ and $P_{D\max}$ parameters that can easily be determined, (2) and (4) lead to explicit optimum solutions for $P_D(\omega_0)$ and $P_G(\omega_0)$ [2], included for later reference:

$$P_{D\text{opt}}(\omega_0)=P_{D\max}\cdot\left(1-\frac{1}{\tilde{\Gamma}(\omega_0)}\right) \tag{5}$$

$$P_{G\text{opt}}(\omega_0)=P_{D\max}\cdot\frac{\ln\tilde{\Gamma}(\omega_0)}{\tilde{\Gamma}(\omega_0)}. \tag{6}$$

Large-signal conjugate matching conditions at the device ports are assumed in these solutions, but the actual values of the corresponding device terminating impedances still remain undefined. In an effort to bypass large-signal measurements altogether, it would be desirable if the missing information could be acquired, again, through the use of empirical approximations. Unfortunately, this is not as easily accomplished as in the case of the power saturation characteristics, where the phase of the signal is not a primary concern. The problem arises from the device parasitics obscuring the intrinsic nonlinear mechanisms in a way which complicates the circuit design and is different for each individual device. The difficulty is resolved by employing a large-signal model to de-embed the intrinsic nonlinearities, resulting in an exceptionally simple composite solution to both the large-signal impedance question *and* the previous optimum feedback problem.

Due to the similarity between nonlinear device operation in power amplifiers and in oscillators, the results obtained in previous amplifier-oriented studies [8], [9] become applicable to the present design effort as well. The model used here, as depicted in the boxed-in portion of Fig. 3, recognizes only nonlinearities associated with the transconductance G_M and the output resistor R_O. These two elements produce the nonlinear fundamental-frequency effects of practical significance. Comprehensive verification of this claim has been provided in [8] based on demonstrated agreement between measurements and model predictions involving three different device geometries.

The values of the linear model elements and the small-signal values of the nonlinear elements are derived from measured small-signal S-parameters using familiar curve-fitting techniques. The model topology in Fig. 3 is, thereby, somewhat more elaborate than is generally required in amplifier applications. The additional complexity stems from the need to more readily distinguish between individual parasitic contributions when the device is used in a configuration that differs from the one employed during initial experimental device characterization. Section V presents an example of such a situation, where a common-drain VCO design is based on a model derived from conventional common-source data.

The main issue is, of course, the assessment of the large-signal behaviors of the nonlinear elements and finding their optimum operating conditions. According to the model definition [8], [9], the instantaneous values for G_M and R_O can be described as time-invariant functions of the voltage across the intrinsic gate capacitor and the voltage across the intrinsic drain-source terminals. With reference to Fig. 3, it thus follows that the mode of oscillation is uniquely determined by three basic parameters, namely the fundamental frequency Fourier components of the two voltages, V_1 and V_2, and the intrinsic load impedance Z_{LL}. By relying on these as principal design variables, the optimum gate-to-drain feedback and optimum load conditions, discussed earlier in terms of device-external power and impedance parameters, lend themselves to a particularly simple and coherent formulation.

C. Optimum Intrinsic Load Impedance

Due to the characteristics of the governing nonlinear mechanisms, the solutions for V_1, V_2, and Z_{LL} are all interrelated and, in principle, cannot be sought independently from one another. Nevertheless, it has been found that an independent approximation can be employed successfully in the case of Z_{LL} without introducing errors of practical significance. The approximation is based on the observation that both nonlinear model elements are resistive in nature and that, hence, the fundamental frequency current I_{GOM} (Fig. 3) through their parallel combination must be exactly out of angular phase with V_2, the voltage across them. To satisfy the resonance requirement at the oscillating frequency ω_0, noting that Z_{LL} includes the drain-source capacitance of the device

$$\text{Im}\{Z_{LL}(\omega_0)\}=0. \tag{7}$$

The functional relationship between the instantaneous value of I_{GOM} and the instantaneous values of V_1 and V_2 fully define the combined nonlinear properties of G_M and R_O. This relationship, when plotted, establishes what has been termed the "dynamic I–V-characteristics" of the intrinsic device [9]. With regard to these characteristics, which are symbolically represented in Fig. 4, $Z_{LL}(\omega_0)$ can be interpreted as describing a *resistive* load line in accordance with (7). At low drive levels the optimum value of

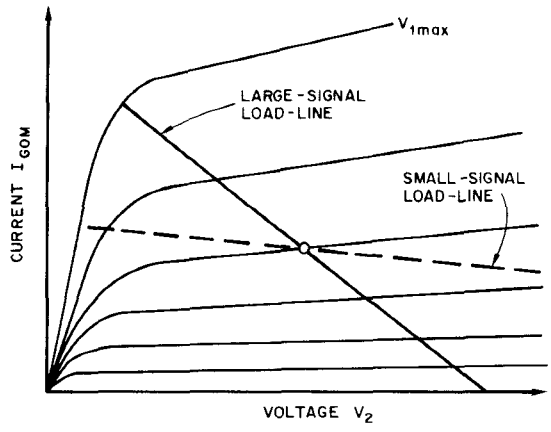

Fig. 4. Large-signal versus small-signal load lines in the $I_{GOM}-V_2$ plane.

$Z_{LL}(\omega_0)$ is equal to the small-signal value of R_O. This value is implicitly used in designs that rely entirely on small-signal device information. The optimum large-signal solution is determined by the value $Z_{LL}(\omega_0)=R_{LL\text{opt}}$ which maximizes the available power at the drain-source port of the device for a given amplitude of V_1. As visualized in Fig. 4, large-signal and small-signal solutions are expected to differ considerably. It is also readily apparent that implementing a resistive value for $Z_{LL}(\omega_0)$ automatically leads to conjugately matched external device ports as prescribed by the resonance condition.

The optimum load-line resistance $R_{LL\text{opt}}$ is a function of drive level, but asymptotically approaches a limit value as the device is driven into saturation. The actual drive level is determined by (2) and typically requires device operation at around 2 to 3 dB of gain compression. The optimum load line under these conditions turns out to be very close to the limit case, suggesting the use of this limit value as an approximation to $R_{LL\text{opt}}$.

For given bias voltages, the limit value corresponds to the load line that yields the maximum product of current swing times voltage swing in the dynamic $I_{GOM}-V_2$ plane, with V_1 varying between the bounds determined by pinch-off and gate forward conduction (Fig. 4). Simple graphical means can be applied to find the asymptotic load line, provided the bounding forward conduction $I_{GOM}-V_2$ curve is known. This curve could be acquired with the quasi-static modeling technique [9], based on four or five small-signal device S-parameter measurements at selected bias-voltage combinations. The approach pursued here, though, is to establish an estimate derived from 1) the measured static device $I_{DS}-V_{DS}$ characteristics, 2) the similarity between these and the dynamic characteristics [9], and 3) the knowledge of the small-signal values of the resistive model elements at the nominal bias point. The errors experienced when relying on this estimate for determining the asymptotic load-line impedance prove to be relatively insignificant when compared to uncertainties arising from typical spread in device characteristics. This assertion is supported by both of the oscillator examples investigated in detail later, whose designs rely on this approximation.

D. Optimum Intrinsic Voltage Feedback Conditions

The next step is to derive optimum values for V_1 and V_2, $V_{1\text{opt}}$ and $V_{2\text{opt}}$, that satisfy the feedback condition (2). This is accomplished by relying on the solutions (5) and (6) given in terms of device-external power levels and relating these to the intrinsic voltage variables V_1 and V_2. As for the conditions at the conjugately matched drain port of the device (Fig. 1), the optimum power level $P_{D\text{opt}}$ to be substituted into (5) can be written as

$$P_{D\text{opt}}(\omega_0)=\gamma\cdot\frac{|V_{2\text{opt}}(\omega_0)|^2}{R_{LL\text{opt}}}. \tag{8}$$

The proportionality factor γ can be estimated based on knowledge of the small-signal model parameters. Neglecting drain-to-gate feedback yields (Fig. 3)

$$\gamma\approx\frac{R_{LL\text{opt}}-R_S-R_D}{R_{LL\text{opt}}} \tag{9}$$

as a viable working assumption. The saturated value of $P_{D\text{opt}}(\omega_0)$ is determined by $V_{2\max}$, the square-wave peak-to-peak voltage swing of V_2 along the $R_{LL\text{opt}}$ load line as constrained by pinch-off and forward conduction of the Schottky barrier:

$$P_{D\max}\approx\gamma\cdot\frac{2}{\pi^2}\cdot\frac{V_{2\max}^2}{R_{LL\text{opt}}}. \tag{10}$$

Device–circuit interaction at the gate port is known to be essentially power-independent, leading to a proportionality between $P_{G\text{opt}}$ and $|V_{1\text{opt}}|^2$ analogous to (8). Although the exact relationship can, of course, be calculated in a straightforward way from the small-signal device model, it can also be approximated, for practical purposes, by

$$P_{G\text{opt}}(\omega_0)=\gamma\cdot\tilde{G}_M^2\cdot\left(\frac{\tilde{R}_O\cdot R_{LL\text{opt}}}{\tilde{R}_O+R_{LL\text{opt}}}\right)^2\cdot\frac{1}{\tilde{\Gamma}(\omega_0)}\cdot\frac{|V_{1\text{opt}}(\omega_0)|^2}{R_{LL\text{opt}}} \tag{11}$$

with $\tilde{G}_M$ and $\tilde{R}_O$ the previously determined small-signal values for transconductance and drain-source resistance,

respectively (Fig. 3). Substituting (8), (10), and (11) into (5) and (6), while also taking the time-delay τ (Fig. 3) into account, yields

$$V_{2\text{opt}}(\omega_0)=\frac{\sqrt{2}}{\pi}\cdot V_{2\max}\cdot\sqrt{1-\frac{1}{\tilde{\Gamma}(\omega_0)}}\cdot e^{-j\omega_0\tau} \quad (12)$$

and

$$V_{1\text{opt}}(\omega_0)=\frac{\sqrt{2}}{\pi}\cdot V_{2\max}\cdot\frac{1}{\tilde{G}_M}\cdot\frac{\tilde{R}_O+R_{LL\text{opt}}}{\tilde{R}_O\cdot R_{LL\text{opt}}}\cdot\sqrt{\ln\tilde{\Gamma}(\omega_0)} \quad (13)$$

whereby the phase angle of $V_{1\text{opt}}$ has arbitrarily been set equal to zero. These solutions are implicitly based on the interrelationship between V_1 and V_2, represented by

$$|V_2|=\frac{\sqrt{2}}{\pi}\cdot V_{2\max}\cdot\sqrt{1-\exp\left\{-\frac{\pi^2}{2}\cdot\left(\tilde{G}_M\cdot\frac{\tilde{R}_O\cdot\tilde{R}_{LL\text{opt}}}{\tilde{R}_O+R_{LL\text{opt}}}\cdot\frac{|V_1|}{V_{2\max}}\right)^2\right\}}. \quad (14)$$

It is noted that this postulated expression is independent of device parasitic effects, unlike the approximation (4) which (14) replaces.

E. Synthesis of Optimum Coupling Network

Once the values of Z_{LL}, V_1, and V_2 have been defined in accordance with the preceding outline, the device-external voltages and currents V_D, V_G, I_D, and I_G, are fixed. Their values can be calculated from the model by way of a sequence of simple variable substitutions into Kirchhoff equations. The model topology permits these substitutions to be carried out without the need for an explicit matrix inversion. Assuming, again, the coupling network in Fig. 1 to be lossless, the power delivered to the 50-Ω external load then follows from (1), noting the current direction convention used in Fig. 3

$$P_{\text{load}}(\omega_0)=\text{Re}\{V_D(\omega_0)\cdot I_D^*(\omega_0)\}+\text{Re}\{V_G(\omega_0)\cdot I_G^*(\omega_0)\}. \quad (15)$$

Due to having neglected, in effect, parasitic feedback internal to the device when deriving (12) and (13), expression (15) will give a value for P_{load} that falls slightly short of the actual maximum. The deviation is typically of the order of 0.5 dB. The true optimum can be sought by repeating the evaluation of (15) for a series of perturbed values of $V_{1\text{opt}}$ and $V_{2\text{opt}}$ consistent with (14). This simple iterative procedure was used in both of the oscillator examples to be discussed.

The next step is to derive coupling network configurations that satisfy the boundary conditions specified in terms of the prescribed voltages and currents at the external device ports. Minimum complexity networks that provide the required four degrees of freedom contain three lumped circuit elements in the form of two reactances and one (lossy) complex element. The elements can be arranged either in a T- or a Π-configuration, thereby defining a two-port prototype of the actual three-port coupling network. An example of a T-configuration is indicated in Fig. 3. The lossy element, which implicitly accounts for the external 50-Ω load in the actual circuit, can in principle occupy any one of the three possible locations in either of the prototype circuits. The resulting generality permits essentially all oscillator design alternatives of practical interest to be treated in a simple unified way. Also, it should be noted that the approach can easily be adapted to include configurations which do not fit the basic T or Π format.

TABLE I
PROTOTYPE ELEMENT VALUES FOR T-CONFIGURATION

CASE	Z_G	Z_S	Z_D
$\text{Re}\{Z_G\}=\text{Re}\{Z_S\}=0$	$j\,\frac{\text{Re}\{V_G\cdot(I_G^*+I_D^*)\}}{\text{Im}\{I_G^*\ I_D\}}$	$j\,\frac{\text{Re}\{V_G\ I_G^*\}}{\text{Im}\{I_G\ I_D^*\}}$	$\frac{V_D}{I_D}-Z_S\left(1+\frac{I_G}{I_D}\right)$
$\text{Re}\{Z_G\}=\text{Re}\{Z_D\}=0$	$j\,\frac{\text{Re}\{I_D\ (V_D^*-V_G^*)\}}{\text{Im}\{I_G\cdot I_D^*\}}$	$\frac{V_G-Z_G\ I_G}{I_G+I_D}$	$j\,\frac{\text{Re}\{I_G\ (V_G^*-V_D^*)\}}{\text{Im}\{I_D\cdot I_G^*\}}$
$\text{Re}\{Z_S\}=\text{Re}\{Z_D\}=0$	$\frac{V_G}{I_G}-Z_S\left(1+\frac{I_D}{I_G}\right)$	$j\,\frac{\text{Re}\{V_D\cdot I_D^*\}}{\text{Im}\{I_D\ I_G^*\}}$	$j\,\frac{\text{Re}\{V_D\ (I_D^*+I_G^*)\}}{\text{Im}\{I_D^*\ I_G\}}$

TABLE II
PROTOTYPE ELEMENT VALUES FOR Π-CONFIGURATION

CASE	Y_{GS}	Y_{GD}	Y_{DS}
$\text{Re}\{Y_{GS}\}=\text{Re}\{Y_{GD}\}=0$	$j\,\frac{\text{Re}\{I_G\ (V_D^*-V_G^*)\}}{\text{Im}\{V_G^*\ V_D\}}$	$j\,\frac{\text{Re}\{I_G\ V_G^*\}}{\text{Im}\{V_G^*\ V_D\}}$	$\frac{I_D}{V_D}+Y_{GD}\left(\frac{V_G}{V_D}-1\right)$
$\text{Re}\{Y_{GS}\}=\text{Re}\{Y_{DS}\}=0$	$\frac{\text{Re}\{V_D\ (I_D^*+I_G^*)\}}{\text{Im}\{V_G^*\ V_D\}}$	$\frac{Y_{GS}\ V_G-I_G}{V_D-V_G}$	$j\,\frac{\text{Re}\{V_G\ (I_G^*+I_D^*)\}}{\text{Im}\{V_D^*\ V_G\}}$
$\text{Re}\{Y_{GD}\}=\text{Re}\{Y_{DS}\}=0$	$\frac{I_G}{V_G}+Y_{GD}\cdot\left(\frac{V_D}{V_G}-1\right)$	$j\,\frac{\text{Re}\{I_D\ V_D^*\}}{\text{Im}\{V_D^*\ V_G\}}$	$j\,\frac{\text{Re}\{I_D\ (V_G^*-V_D^*)\}}{\text{Im}\{V_D^*\ V_G\}}$

The actual choice between T- or Π-configuration is primarily determined by the necessity to minimize the number of resonances in the vicinity of ω_0 in order to avoid parasitic oscillation effects. The choice is particularly crucial in broad-band VCO designs. For gate and drain operating near series resonance, for instance, the series-element T-configuration is generally preferred. This situation normally occurs when using devices in chip form. The decision of where to position the lossy element within the chosen topology is guided by physical realizability considerations. The decision process is aided by the ease with which the method allows the possible alternatives to be evaluated and their individual merits to be compared. The expressions for calculating the prototype element values from the optimum values for V_D, V_G, I_D, and I_G (Fig. 5) are summarized in Tables I and II.

The final step in the design procedure is the physical implementation of the prototype network. This step is simple in a lumped-element design as might be required for monolithic realization. The next section shows an example of a distributed implementation, while a semilumped circuit is discussed in Section V.

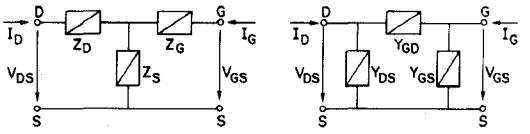

Fig. 5. The two basic prototype topologies.

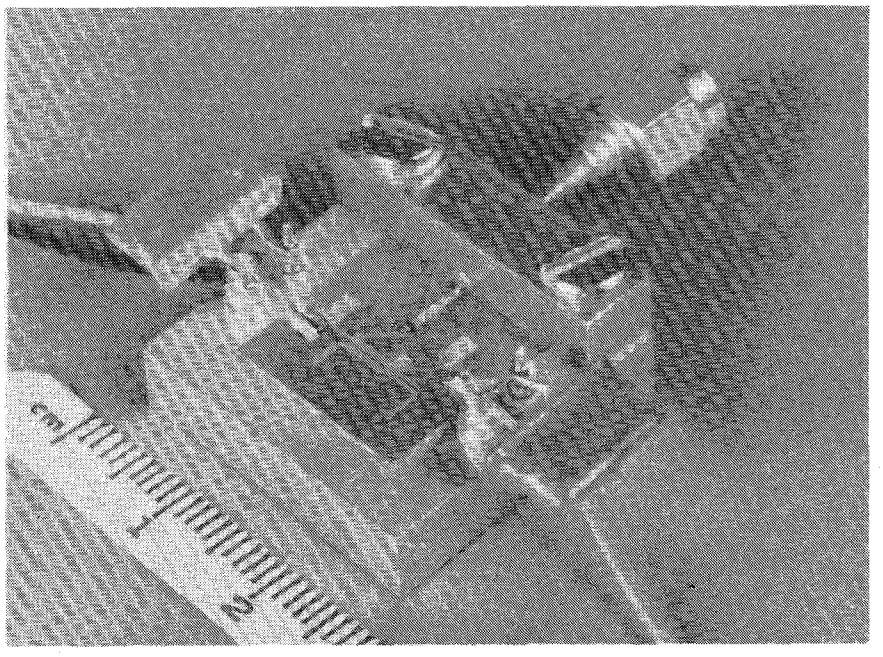

Fig. 6. Experimental 17-GHz GaAs FET oscillator with distributed element coupling network.

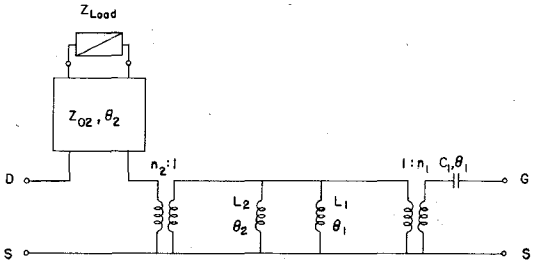

Fig. 7. Equivalent circuit of distributed 17-GHz coupling network.

III. A 17-GHz Fixed-Frequency Oscillator Example

To demonstrate the viability of the technique, the described procedure has been applied to the design of a 17-GHz fixed-frequency oscillator. Its distributed element implementation, realized as a coupled-line microstrip circuit on a 0.25-mm Duroid substrate, is depicted in Fig. 6. The design is based on a T-prototype with the load element in series with the drain lead of the device. The T-configuration is evident from the equivalent distributed circuit of the coupling network shown in Fig. 7, in which inductors and capacitors symbolize short-circuited and open-circuited stubs of electrical lengths θ_1 and θ_2, respectively, in accordance with the notation introduced by Wenzel [10]. The distributed design offers more degrees of freedom than are actually required. This flexibility can be utilized to accommodate physical realizability constraints without adding new undesirable system resonances in the vicinity of the oscillating frequency.

The device employed in the circuit is a single cell of an Avantek M110 device [11] having a 0.5-μm$\times$375-μm gate geometry. With the transistor biased for operation at a drain-source voltage of 4 V and a drain current of $0.6 \cdot I_{DSS}$, the design theory estimates the 17-GHz RF output power from the oscillator at 18 dBm, based on an optimum intrinsic load-line resistance $R_{LL\text{opt}} = 50\ \Omega$. The estimate is in close agreement with the measured performance of the actual oscillator, yielding a maximum of 17.5 dBm of output power with 21-percent efficiency at a drain-source bias voltage of 3.8 V. By lowering the voltage to 3.0 V the efficiency increased to 25 percent while the output power dropped to 16.5 dBm. As predicted, the frequency selectivity of the distributed coupling network, in conjunction with two supplementary RC damping elements added to the

gate and drain bias circuits, effectively suppressed all parasitic oscillations.

IV. Design of Voltage-Controlled Oscillators

The optimum design of a voltage-controlled oscillator involves meeting the criteria developed in Section II at each tuned oscillating frequency within the band of interest. This leads, in terms of prototype circuit elements, to uniquely prescribed frequency responses of their impedance values. The individual impedance functions are determined through repeated implementation of the fixed-frequency procedure for a representative set of frequency samples covering the anticipated tuning bandwidth. The choice of prototype configuration warrants particular scrutiny. This choice becomes crucial in wideband applications where it is important to rule out in-band antiresonances that could introduce frequency jumping and hysteresis effects in the tuning characteristics. Equal care must be devoted, of course, to preserving essential prototype characteristics during the physical implementation of the oscillator circuit.

Independent of prototype configuration, the required frequency responses of the two prototype reactances generally exhibit negative slopes. Voltage-controlled elements, such as varactors or YIG-devices, are hence needed to satisfy the reactance requirements. For the sake of simplicity, the present discussion concentrates on varactor-tuned circuits for situations where frequency agility is essential, although the approach can be applied just as easily to the design of YIG-tuned oscillators. For both types of tuning it is important to note that optimum exploitation of transistor power-bandwidth capabilities will normally call for *two* separate tuning elements. This is illustrated with the VCO example detailed in Section V which demonstrates that substantial performance degradation results if tuning is confined to merely one circuit element.

The tuning bandwidth achievable with a specific transistor is primarily determined by the ranges of reactance values that can be spanned for given maximum varactor capacitance variation, and by the constraints associated with the physical implementation of the lossy load-related prototype element. An obvious approach to realizing the load element is to synthesize its prescribed optimum impedance function as the driving point impedance of a lossless two-port network terminated in the external 50-Ω load resistor. This problem can be solved with conventional matching techniques. As for the tuning reactances, they should preferably be implemented in lumped-element form to preserve bandwidth. In practice this is accomplished by using lengths of bond wire or other types of lumped inductors to resonate varactor capacitances. The combination of varactor and inductor(s) is chosen so that the total reactance $X_T(\omega_0)$ exhibits smooth tunability within the frequency tuning interval $\omega_L \leq \omega_0 \leq \omega_H$ in accordance with the range of reactance values specified by the prototype. In realizing a series connected prototype reactance, augmentation of the varactor with a series inductor will normally be called for, with the dual thereof applying to a parallel connected prototype element. Three examples are illustrated in Fig. 8, in each of which L_A represents the external inductor and L_B accounts for an assumed fixed minimum lead inductance associated with the varactor chip. For calculation purposes, it is easiest to lump varactor losses with the transistor part of the circuit. With a maximum achievable varactor capacitance ratio $\rho_{\max} = C_{V\max}/C_{V\min}$, and specified limit values $X_T(\omega_L)$ and $X_T(\omega_H)$, the inductor L_A, and the relationship between varactor capacitance C_V and angular oscillating frequency ω_0 for the series type circuit in Fig. 8(a) must be chosen according to

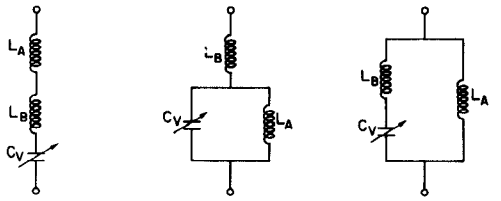

Fig. 8. Lumped-element realizations of varactor-tuned reactances.

$$L_A = \frac{\omega_L \cdot \rho_{\max} \cdot X_T(\omega_L) - \omega_H \cdot X_T(\omega_H)}{\omega_L \cdot \omega_H \cdot ((\omega_L \cdot \rho_{\max}/\omega_H) - (\omega_H/\omega_L))} - L_B \geq 0 \tag{16}$$

$$C_V(\omega_0) = \frac{1}{\omega_0 \cdot (\omega_0 \cdot L_A + \omega_0 \cdot L_B - X_T(\omega_0))}, \quad \omega_L \leq \omega_0 \leq \omega_H. \tag{17}$$

The analogous expressions for the parallel resonated circuit in Fig. 8(b) are

$$L_A = \frac{(\omega_L \cdot \rho_{\max}/\omega_H) - (\omega_H/\omega_L)}{(\omega_H/(X_T(\omega_L) - \omega_L \cdot L_B)) - (\omega_L \cdot \rho_{\max}/(X_T(\omega_H) - \omega_H \cdot L_B))} \geq 0 \tag{18}$$

$$C_V(\omega_0) = \frac{1}{\omega_0} \cdot \left(\frac{1}{X_T(\omega_0) - \omega_0 \cdot L_B} + \frac{1}{\omega_0 \cdot L_A} \right), \quad \omega_L \leq \omega_0 \leq \omega_H. \tag{19}$$

For the circuit in Fig. 8(c) one obtains

$$L_A = \frac{1}{P \pm \sqrt{P^2 - Q}} \geq 0 \tag{20}$$

$$C_V(\omega_0) = \frac{1}{\omega_0} \cdot \left(\omega_0 \cdot L_B - \frac{1}{(1/X_T(\omega_H)) - (1/(\omega_0 \cdot L_A))} \right)^{-1}, \quad \omega_L \leq \omega_0 \leq \omega_H \tag{21}$$

with

$$P = \frac{1}{2} \cdot \left\{ \frac{\omega_L}{X_T(\omega_L)} + \frac{\omega_H}{X_T(\omega_H)} - \frac{1}{L_B} \right\}$$

$$Q = \frac{\omega_L \cdot \omega_H}{X_T(\omega_L) \cdot X_T(\omega_H)} - \frac{1}{L_B} \cdot \frac{(\omega_H/X_T(\omega_L)) - (\omega_L \cdot \rho_{\max}/X_T(\omega_H))}{(\omega_H/\omega_L) - (\omega_L \cdot \rho_{\max}/\omega_H)}.$$

Naturally, situations also arise where (16)–(21) indicate the need for supplementing the varactor with a capacitor rather than an inductor. The net effect is to reduce the actual capacitance variation. The simplest solution involves relaxing the requirements on $\rho_{\max}$ by utilizing only part of the total available capacitance variation ρ according to

$$\rho=\frac{\omega_H\cdot(X_T(\omega_H)-\omega_H\cdot L_B)}{\omega_L\cdot(X_T(\omega_L)-\omega_L\cdot L_B)}<\rho_{\max} \tag{22}$$

and

$$C_V(\omega_0)=\frac{1}{\omega_0\cdot(\omega_0\cdot L_B-X_T(\omega_0))},\qquad \omega_L\leqslant\omega_0\leqslant\omega_H. \tag{23}$$

In assessing the limitations associated with the varactors it should be observed that RF varactor voltage swings in practical oscillator circuits can be quite large. It is thus essential to adequately account for the large-signal varactor properties, which can be accomplished through direct large-signal impedance measurements [12]. The chief consequence of elevated RF drive is to lower the effective varactor capacitance value and to increase losses, whereby the discrepancies between small-signal and large-signal values are most apparent for bias voltages at which the RF voltage starts swinging into the forward bias region. When compared to predictions based solely on small-signal varactor characteristics supplied by the manufacturer, this translates into reduced tuning bandwidth, particularly at the low end.

The optimum RF power level achievable for each frequency setting decreases with increasing frequency due to transistor gain rolloff. However, if merely an overall lower limit on output power is specified, it is possible to trade excess power available at the lower frequencies against additional bandwidth and relaxed physical realization constraints. This can be accomplished by allowing both the intrinsic load-line resistance and the intrinsic voltage feedback ratios to deviate from their respective calculated optimum values $R_{LL\text{opt}}$ and $V_{2\text{opt}}(\omega_0)/V_{1\text{opt}}(\omega_0)$, $\omega_L\leqslant\omega_0\leqslant\omega_H$. A numerical optimization scheme analogous to the one applied to the design of a negative resistance VCO [13] can be employed to assist in the tradeoff evaluation. This approach has not been pursued in the present investigation. Rather, the example described in the following section illustrates how possible tradeoffs can be assessed and implemented without the need for sophisticated computational tools.

V. Example of a Broad-Band Varactor-Tuned Oscillator

The goal set for this example was to achieve a flat output power response over the frequency range from 8.0 to 12.0 GHz utilizing the 750-μm total gate width of the two-cell 0.5-μm gate-length Avantek device [11]. Both T- and Π-type configurations were investigated, applying the procedure outlined in the previous section. All Π-type solutions disqualified themselves because of in-band antiresonances.

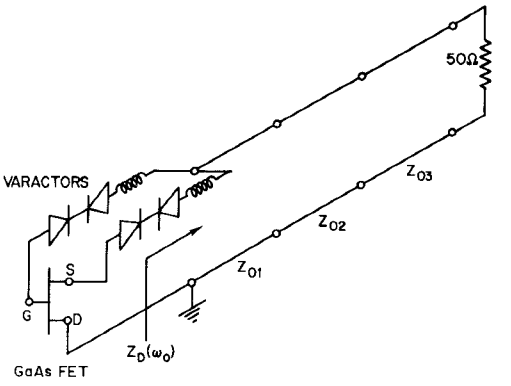

Fig. 9. Schematic of broad-band tunable oscillator circuit.

The T-configuration with the load-element in series with the gate of the device was also discarded due to severe tuning bandwidth limitations dictated by the pertinent realizability constraints. Between the two remaining feasible T-type alternatives the one with the load element in series with the drain lead appeared most attractive.

A schematic of the chosen overall circuit concept is shown in Fig. 9. The prototype load element is synthesized as a cascade of three transmission line elements terminated in 50 Ω. The drain of the device is grounded to facilitate realization in microstrip. Each of the two tuning elements contains a series combination of two individual varactors, in order to use commercially available Microwave Associates MA 46629 hyperabrupt varactor chips and still achieve the low capacitance values associated with wide-band tunability. To preserve bandwidth, lumped inductors are employed, implemented in the form of interconnecting bond wires.

Designing an oscillator to maintain the optimum intrinsic load impedance $R_{LL\text{ opt}}$ at all frequencies within the band can be accomplished, as discussed previously, by calculating the corresponding prototype element impedance responses and correlating them with physical realizability. If tradeoffs are to be considered, the calculations must be repeated for a representative number of values of $R_{LL}\gtrless R_{LL\text{opt}}$ and $V_2/V_1\gtrless V_{2\text{opt}}/V_{1\text{opt}}$. The compilation of the data can be accomplished very efficiently due to the simplicity of the individual analyses. A set of mutually compatible solutions is then chosen from the data so as to establish prototype frequency characteristics in accordance with the tradeoff objectives. For a given prototype configuration and given technological limits on minimum varactor size, tradeoffs involving the physical implementation of the load element are generally the primary contributors to design flexibility. To illustrate this, the prototype load element impedance for the present VCO example has been plotted in Fig. 10(a) and 10(b) as a function of frequency F and intrinsic load-line resistance R_{LL} for two specific values of V_2/V_1. The response yielding maximum RF power at each frequency setting corresponds to the locus for $R_{LL}=R_{LL\text{opt}}=30\ \Omega$ in Fig. 10(b). Also indicated in Fig. 10(b) is the more readily implemented characteristic labeled Z_D which represents the driving point impedance of the

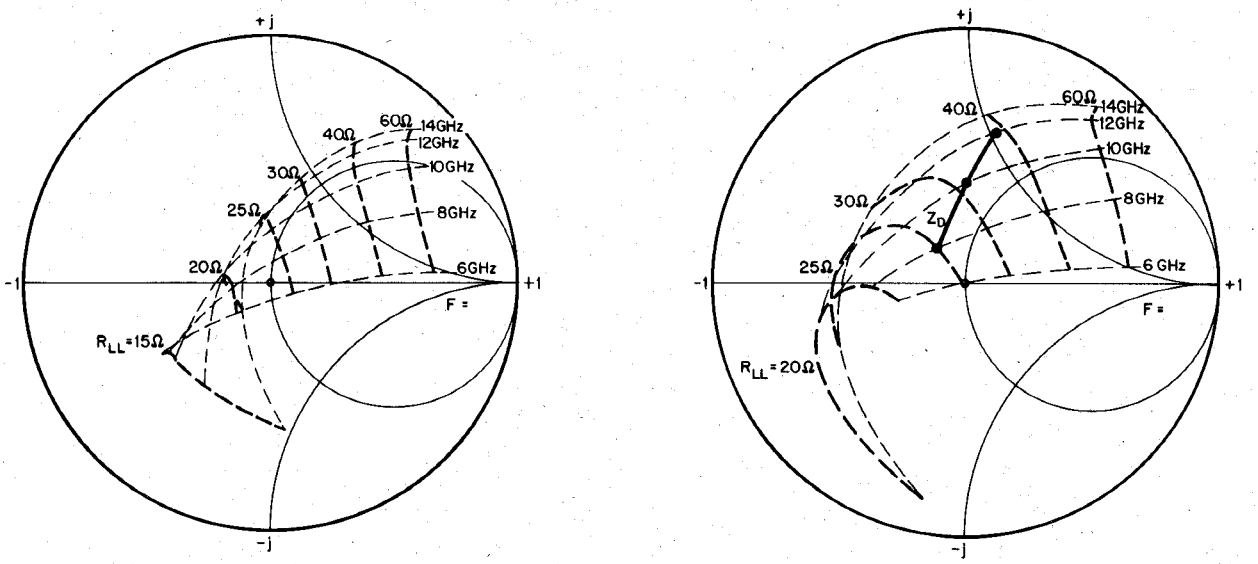

Fig. 10. Prototype load impedance Z_D, normalized to $Z_0 = 10\ \Omega$, as a function of frequency F and load-line resistance R_{LL}. (a) $V_2/V_1 = 0.8 \cdot V_{2\text{opt}}/V_{1\text{opt}}$. (b) $V_2/V_1 = V_{2\text{opt}}/V_{1\text{opt}}$.

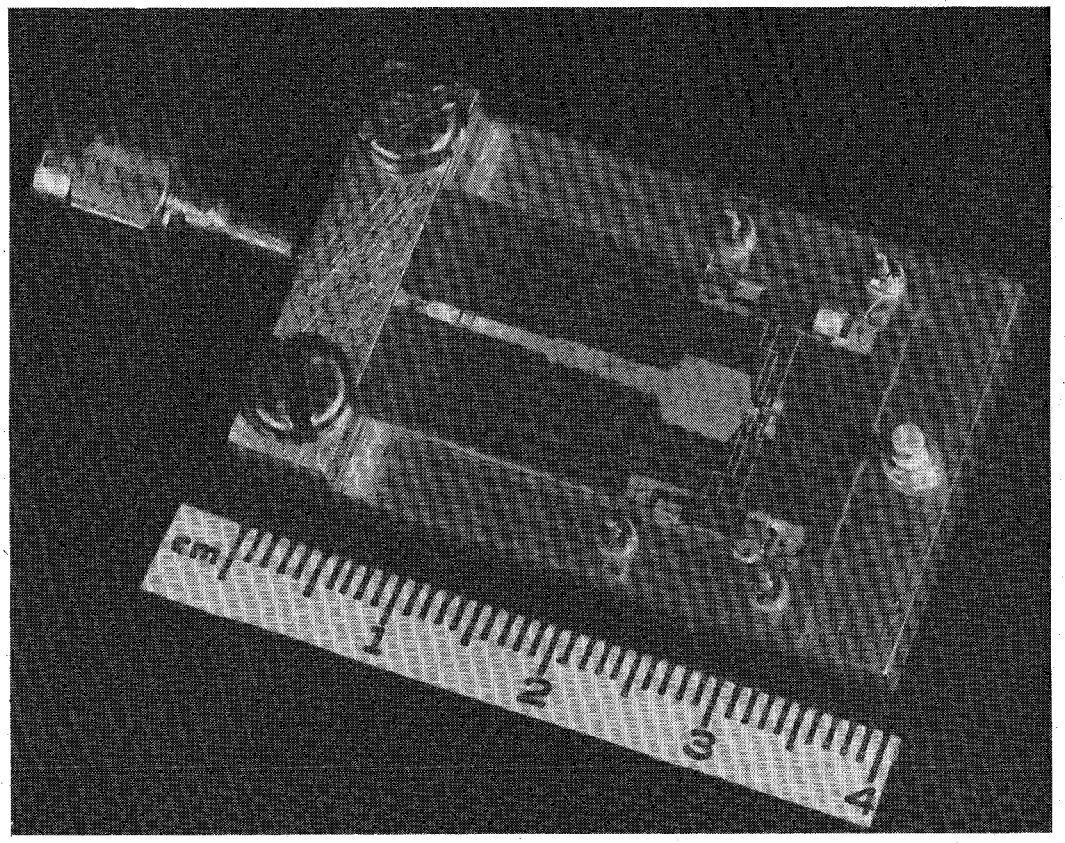

Fig. 11. Varactor-tuned 7.4- to 13.1-GHz GaAs FET oscillator.

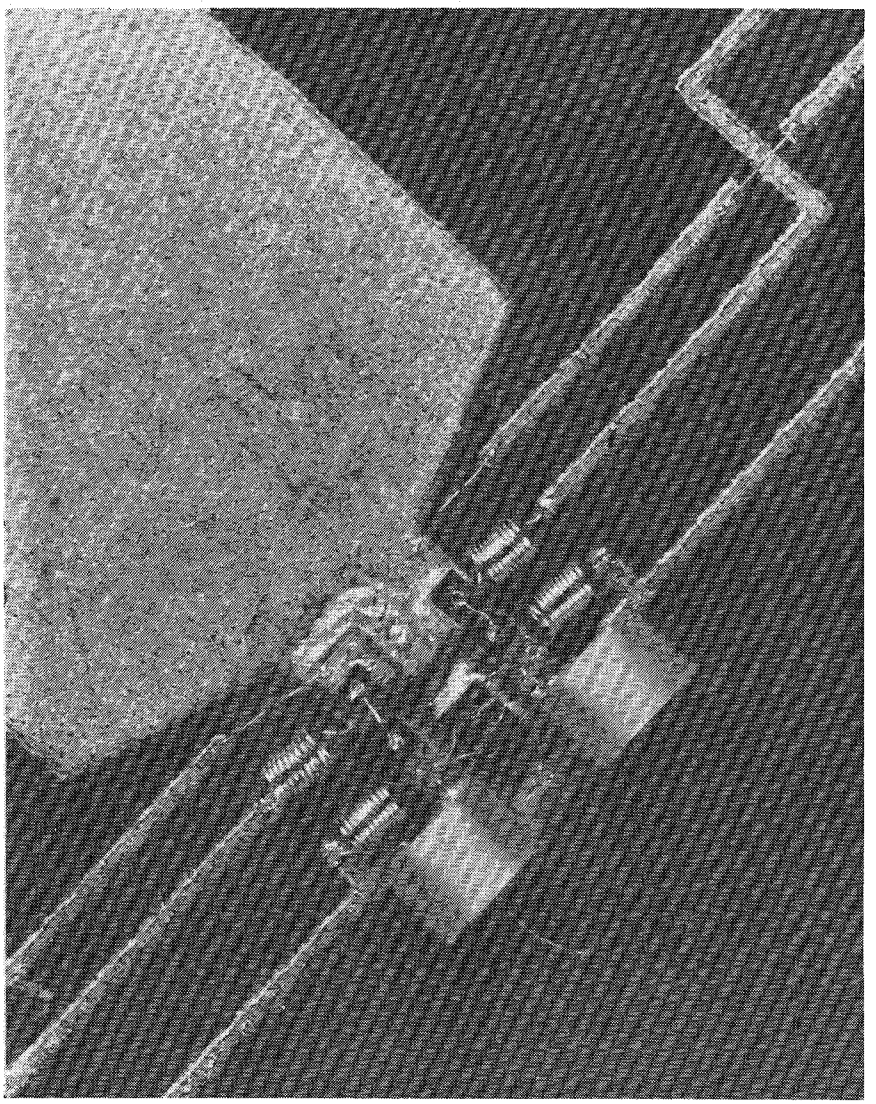

Fig. 12. Close-up view of transistor and dual tuning arrangement.

cascaded transmission line structure indicated in Fig. 9. Improved realizability was achieved through sacrifice of only 0.5 dB in minimum output power, while flattening the output power versus frequency response at the same time.

The actual oscillator circuit, built on a 0.25-mm Duroid substrate, is depicted in Fig. 11. A close-up view of the immediate vicinity of the transistor and the tuning arrangement is given in Fig. 12. The miniature 0.3-mm diameter choke coils, consisting of ten turns of 25-μm diameter gold wire, supply the bias voltages to the transistor and the varactors. The coils are connected to RF short-circuited high impedance quarter-wavelength stubs to form a broadband composite bias circuit. Effective in-band safeguarding against spurious oscillations is accomplished by adding a 50-Ω resistor in parallel with the bias chokes at gate and source.

The oscillator design is based on a conservative maximum capacitance ratio $C_{V\max}/C_{V\min}$ of 6:1. The reason for this conservative assumption was to provide enough built-in latitude in order to obtain the specified 8.0- to 12.0-GHz bandwidth without involving post-design tweaking of the circuit. (This would have called for replacing bond wires which was judged impractical.) The capacitance ratios of the actual varactors used were in excess of 6:1, providing a larger tuning interval than initially specified, namely from 7.4 to 13.1 GHz. Measured and predicted RF output power responses are given in Fig. 13, together with the associated gate and source varactor tuning voltages V_{VG} and V_{VS}, respectively. The agreement between experiment and prediction is judged to be well within the range of uncertainty determined by spread in device characteristics and circuit tolerances.

The main purpose of the example has been to verify the viability of the design technique rather than to demonstrate, for instance, maximum bandwidth capabilities. It was noted, however, that disconnecting the two 50-Ω stabilizing resistors increased the tuning range by an additional 500 MHz. This did not impair smooth tunability as long as the varactor bias voltages tracked monotonically according to Fig. 13. However, unlike the situation with the stabilizing resistors in place, the signal exhibited a tendency to "break up" at midband frequencies when the tracking criterion was relaxed.

The present technique is based on the observation that

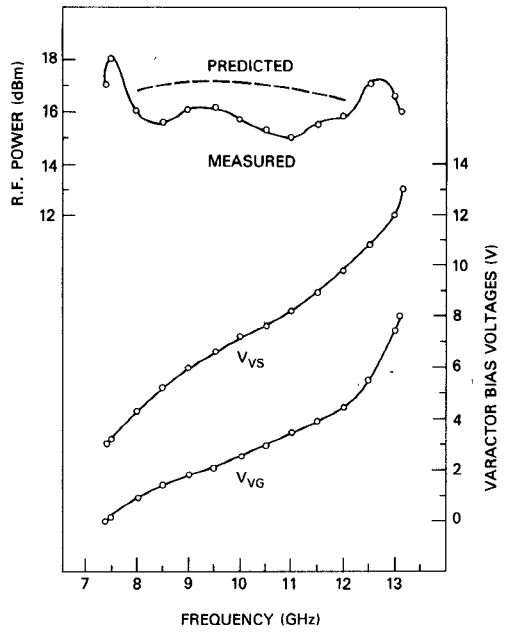

Fig. 13. Measured and predicted RF output power performance, together with associated gate and source varactor tuning voltages V_{VG} and V_{VS}, respectively.

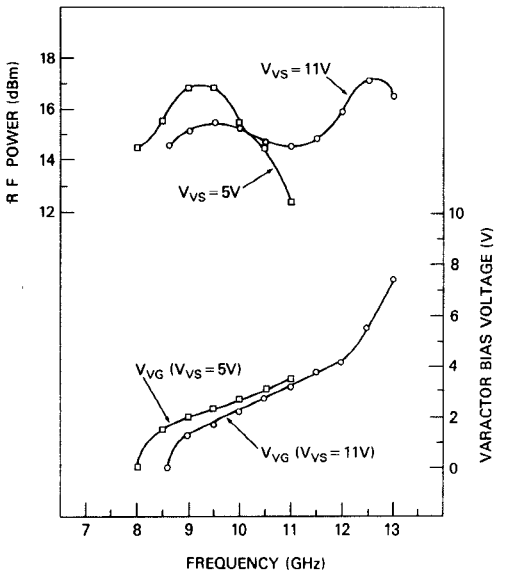

Fig. 14. Measured tuning characteristics for fixed values of source varactor tuning voltage V_{VS}.

two independent tuning elements are needed to obtain optimum performance with a given transistor. In order to assess the actual impact of the approach described here, a conventional single element tuning arrangement was simulated by holding V_{VS} fixed, while varying only the more frequency sensitive gate varactor bias voltage V_{VG}. Fig. 14 shows the tuning characteristics of the oscillator with the source varactor biased at $V_{VS}=5$ V and $V_{VS}=11$ V, respectively. The bandwidth in the latter case spanned 8.6 to 13.0 GHz, representing the *maximum* frequency range obtainable when restricted to tuning only at the gate. Thus, in this particular experiment, using *two* tuning elements as opposed to *one* leads to an increase in bandwidth of 30 percent. Even though this remains an isolated test example, it nevertheless provides insight into the practical significance of the role played by the second tuning element.

VI. Conclusions

A generalized approach to designing GaAs FET oscillators has been described. Among the distinguishing features are its reliability in predicting large-signal oscillator performance and the underlying simplicity of the overall procedure. The crux of the method is to de-embed the nonlinearities of the transistor with the help of a circuit-type model, leading to a concise formulation of optimum oscillating conditions in terms of intrinsic voltage and current variables. It has been demonstrated that the essential information regarding device nonlinearities can be adequately

reconstructed, for practical purposes, from the static I_{DS}–V_{DS} curves and the small-signal model of the device. This provides an attractive alternative to deriving the information from actual large-signal measurements. The technique has been successfully applied to the design of a fixed-frequency and a broad-band varactor-tuned oscillator, yielding good agreement between predictions and experiments. In the case of the varactor-tuned circuit it has been shown, in particular, that two independent tuning elements are indeed essential if the power-bandwidth capabilities of the transistor are to be fully exploited, whereby the same arguments apply to YIG-tuned circuits.

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10-GHz 10-W Internally Matched Flip-Chip GaAs Power FET's

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***Abstract*—A newly developed internally matched configuration for a flip-chip GaAs power field effect transistor is presented. In this structure, gate and drain electrodes of the FET chips are directly connected to the lumped dielectric capacitors in the matching networks by thermocompression bonding using no wire. A power output of 10 W with 3-dB gain and a power added efficiency as high as 14 percent has been realized at 10 GHz.**

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I. INTRODUCTION

RECENT advances in GaAs field effect transistor technology have steadily improved the power output and power gain capabilities of the device over the frequency range from *S*- to *Ku*-band [1]. Nowadays, solid-state power GaAs FET amplifiers are extensively used in telecommunication and phased array radar systems [2], [3]. High power output levels in the *X*-band frequency range are demanded for these applications.

For obtaining higher power output, various types of

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